What is claimed is:

1. A method for optimizing the timing performance of an overall logic circuit where that overall logic circuit is implemented in a Field Programmable Gate Array (FPGA) with programmable interconnect of the FPGA behaving in a way such that the timing of logic signals routed by the programmable interconnect from a specific source to a specific load within the FPGA is affected negligibly by fanout to other logic loads connected to the same source signal, the method comprising the steps of:

a) synthesizing the overall logic for first implementation in an FPGA, the synthesis including construction and first placement of the logic functions on the FPGA,

b) analyzing the timing of the first implementation with the first placement,

c) determining the most critical timing paths from analysis of the first implementation,

d) selecting as an object for improvement a specific critical path from the most critical timing paths,

e) implementing in another way the critical logic in the chosen critical path with implementation of the critical logic performed with relative

disregard as to the fanout of signals to other logic in the overall logic circuit and with placement of logic in the chosen critical path designed primarily to minimize the interconnected routing distance of the signals contributing to that chosen critical path.

2. The method of Claim 1 in which the implementation of the critical logic in a new way in step e) is limited only to changes in the placement of the logic in the chosen critical path.

3. A method for optimizing the timing performance of an overall logic circuit where that overall logic circuit is implemented in an FPGA with programmable interconnect of the FPGA behaving in a way such that the timing of logic signals routed by the programmable interconnect from a specific source to a specific load within the FPGA is affected negligibly by fanout to other logic loads connected to the same source signal, the method comprising the steps of:

a) synthesizing the overall logic for a base implementation in an FPGA, the synthesis including construction and placement of the logic functions on the FPGA,

b) analyzing the timing of the base implementation,

c) determining the most critical timing paths from analysis of the base implementation,

d) selecting as an object for improvement a chosen critical path from the most critical timing paths,

e) implementing in another way the critical logic in the chosen critical path with implementation of the critical logic performed with relative disregard as to the fanout of signals to other logic in the overall logic circuit and with placement of logic in the chosen critical path designed primarily to minimize the interconnected routing distance of the signals contributing to that chosen critical path,

f) modifying the placement of other logic in the overall logic circuit to accommodate the changes in placement of the chosen critical path while maintaining approximately the new placement of the critical logic,

g) repeating steps b) through f) where the last implementation and placement of the overall logic circuit from step f) becomes the basis for starting again with this last implementation becoming the base implementation.

4. The method of Claim 3 in which the implementation of the critical logic in a new way in step e) is limited only to changes in the placement of the logic in the chosen critical path.